channel biasing transistor, and a source terminal of the n-channel biasing transistor is connected to a biasing side power source line comprising:

decreasing an electric potential of an output terminal through the electric discharging transistor during a first period, wherein the output terminal is connected to a source terminal of the n-channel amplifying transistor and wherein one of the output terminal and an electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor;

increasing the electric potential of the output terminal through the n-channel amplifying transistor during a second period.

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68. (New )A driving method of a semiconductor device comprising an n-channel amplifying transistor and an n-channel biasing transistor, wherein a drain terminal of the n-channel amplifying transistor is connected to an amplifying side power source line, a source terminal of the n-channel amplifying transistor is connected to a drain terminal of the n-channel biasing transistor, and a source terminal of the n-channel biasing transistor is connected to a biasing side power source line comprising:

decreasing an electric potential of an output terminal through the n-channel biasing transistor during a first period, wherein the output terminal is connected to a source terminal of the n-channel amplifying transistor;

increasing the electric potential of an output terminal through the n-channel amplifying transistor during a second period;

wherein a gate potential of the n-channel biasing transistor during the first period is lager than a gate potential of the n-channel biasing transistor during the second period.

69. (New) A driving method of a semiconductor device comprising an n-channel amplifying transistor, an n-channel biasing transistor, and a bias signal line, wherein a drain terminal of the n-channel amplifying transistor is connected to an amplifying side power source line, a source terminal of the n-channel amplifying transistor is connected to a drain terminal of the n-channel biasing transistor, a source terminal of the n-channel biasing transistor is connected to a biasing side power source line, and a gate terminal of the n-channel biasing transistor is connected to the bias signal line comprising:

decreasing an electric potential of an output terminal through the n-channel biasing transistor during a first period, wherein the output terminal is connected to a source terminal of the n-channel amplifying transistor;

increasing the electric potential of an output terminal through the n-channel amplifying transistor during a second period;

wherein a gate potential of the n-channel biasing transistor during the first period is lager than a gate potential of the n-channel biasing transistor during the second period by a signal generating device connected to the bias signal line.

70. (New) A driving method of a semiconductor device comprising a p-channel amplifying transistor and a p-channel biasing transistor, wherein a drain terminal of the p-channel amplifying transistor is connected to an amplifying side power source line, a source terminal of the p-channel